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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,415	09/22/2003	Gil Vinitzky	P-1912-US1	4391

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,415	VINITZKY, GIL	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/22/03; 1/5/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 are examined.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-8 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-8 clearly recite a method for performing a sequence of Fast Fourier Transform according to a mathematic algorithm. In order for such a claimed method, computer-related process, or a claimed non-specified apparatus implementing the underlined process to be statutory, the claims must include either a step or means that results in a physical transformation outside the computer or a limitation to a practical application. However, it is clear from the claims that the claims merely recite mathematical step or non-specific means for data computation and manipulation in performing a mathematical function. The input is a set of number and output is also a set of number. The claims fail to recite any step or means that results in a physical transformation outside the computer, that includes a limitation to a practical application, or that requires a specific computer to implement the claimed process. Therefore, claims 1-8 are clearly directed to a non-statutory subject matter.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being obvious over Lim et al. (U.S. 6,463,451) in view of Shridhar et al. (U.S. 6,366,937).

Re claim 2, Lim et al. disclose in Figure 6 a method to calculate four results of a Fast Fourier Transform butterfly calculation (abstract and Figure 2 wherein the butterfly operation is defined), the calculation involving real and imaginary cosinusoidal data inputs, real and imaginary sinusoidal data inputs, and real and imaginary coefficients (col. 1 lines 37-47 wherein cosine and sine are involved), the method comprising: adding a first value to a first product of a real sinusoidal data input and a real coefficient and subtracting therefrom a second product of an imaginary sinusoidal data input and an imaginary coefficient to produce a first result ($Re(X_{out})$ in col. 1 line 41); and adding first value to second product and, subtracting therefrom first product to produce a second result ($Re(Y_{out})$ in col. 1 line 45); and adding a second value to a third product of real sinusoidal data input and imaginary coefficient and to a fourth product of imaginary sinusoidal data input and real coefficient to produce a third result ($Im(X_{out})$ in col. 1 line 3); and subtracting from second value third product and fourth product to produce a fourth result ($Im(Y_{out})$ in col. 1 line 46). Lim et al. fail to disclose the FFT is performed in 2 cycles wherein the first and second results are performed in 1st cycle and the third

and fourth results are performed in 2nd cycle. However, Shridhar et al. disclose in Figure 3 and in column 3 lines 10-20 that a device is capable performed a Fast Fourier Transfer in pipelined fashion four floating-point multiplies and additions/subtractions per clock cycle. In addition, the computation for the 4-point FFT above as cited in column 1 lines 35-47 needs only eight floating-point multiplies and several additions/subtractions operations. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to apply and arrange the 4-point FFT to perform within 2 cycles only wherein the first cycle processes four multiplications, two additions, and two subtractions for the first and second results; and the second cycle processes another four multiplications, two additions, and two subtractions for the third and four results using the pipelined instruction device in Shridhar et al.'s invention into Lim et al.'s invention because it would enable to reduce the computation time (col. 1 lines 37-40).

Re claim 1, it has similar limitations cited in claim 2. Thus, claim 1 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 3, Lim et al. further disclose in Figure 6 the first value is a real cosinsoidal data input ($Re(X_{in})$ in col. 1 line 40-45 wherein X is cosinsoidal signal) and second value is an imaginary real cosinsoidal data input ($Im(X_{in})$ in col. 1 line 40-45 wherein X is cosinsoidal signal).

Re claim 4, Lim et al. further disclose in Figure 6 in first cycle: concatenating a rounding constant to a real produce first value; and in second cycle: concatenating

rounding constant to an imaginary cosinusoidal data input to produce second value (86 in Figure 6).

Re claim 5, Lim et al. fail to disclose in Figure 6 in first cycle: multiplying real sinusoidal data input and imaginary coefficient to produce third product; and multiplying imaginary sinusoidal data input and real coefficient to produce fourth product. Shirdhar et al. disclose in Figure 3 a device has multiple multipliers for multiplying multiple input data (e.g. 32, 34, 36, and 38) in pipeline fashion and the pipelined operation is known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add pipelined multiplier for producing third product and fourth product in the first cycle as seen in Shirdhar et al.'s invention into Lim et al.'s invention because it would enable to reduce the computation time (col. 1 lines 37-40) by pipeline multiplying all the products prior.

Re claim 6, Lim et al. fail to disclose in Figure 6 in second cycle: multiplying a real sinusoidal data input of a next butterfly calculation and a real coefficient of next butterfly calculation to produce a first product for next butterfly calculation; and multiplying an imaginary sinusoidal data input of next butterfly calculation and an imaginary coefficient of next butterfly calculation to produce a second product for next butterfly calculation. However, Shirdhar et al. disclose in Figure 3 a device has multiple multipliers for multiplying multiple input data (e.g. 32, 34, 36, and 38) in pipeline fashion and the pipelined operation is known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add pipelined multiplier for producing first product and second product for the next butterfly operation

in the second cycle as seen in Shirdhar et al.'s invention into Lim et al.'s invention because it would enable to reduce the computation time (col. 1 lines 37-40) by pipeline multiplying all the products prior.

Re claim 7, Lim et al. further disclose in Figure 6 writing to memory first result, second result third result and fourth result within two cycles (e.g. 64, 66, 76, and 78 in addition to rationale in rejection 2).

Re claim 8, Lim et al. further disclose in Figure 6 writing first result and third result to memory in a particular cycle (e.g. 64 and 66 respectively) and second result and fourth result to memory in a next cycle (e.g. 76 and 78 respectively).

Re claim 9, it is a DSP claim of claim 1. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 1. In addition, Lim et al. further disclose in Figure 7 a first multiplier (e.g. 46), a first and second three-input arithmetic logic unit (e.g. {52, 54, 58} and {68, 70, 72}). Lim et al. fail to disclose a second multiplier. However, Shirdhar et al. disclose in Figure 3 multiple multipliers including a second multiplier for processing faster FFT. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a second multiplier as seen in Shirdhar et al.'s invention into Lim et al.'s invention because it would enable to reduce the computation time (col. 1 lines 35-40) by producing two product at a time.

Re claim 10, it is a DSP claim of claim 3. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 11, it is a DSP claim of claim 4. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 12, it is a DSP claim of claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, it is a DSP claim of claim 8. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claim 4 of U.S. Patent No. 6,625,630 contain every element of claim 1 of the instant application respectively and as such anticipate claim 1 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896,225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting

where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). "ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 4,501,149 to Konno et al. disclose a micro fracture detector.

b. U.S. Patent No. 3,702,393 to Fuss discloses a cascade digital fast fourier analyzer.

c. U.S. Patent No. 5,042,000 to Baldwin discloses an integral transform method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

November 2, 2004

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